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1 High-performance Java

Cherri Pancake, Christian Lengauer
October 2001 Communications of the ACM, Volume 44 Issue 10
Publisher: ACM

Full text available: pdf(243.29 KB) html(13.07 KB) Additional Information: full citation, cited by, index terms

2 Lightweight Implementation of the POSIX Threads API for an On-Chip MIPS Multiprocessor with VCI Interconnect

Frederic Petrot, Pascal Gomez
March 2003 DATE '03: Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2, Volume 2
Publisher: IEEE Computer Society

Full text available: pdf(132.95 KB) Publisher Site Additional Information: full citation, abstract, references, cited by, index terms

This paper relates our experience in designing from scratch a multi-threaded kernel for a MIPS R3000 on-chip multiprocessor. We briefly present the target architecture build around a VCI compliant interconnect, and the CPU characteristics. Then we focus ...

3 A novel synthesis technique for communication controller hardware from declarative data communication protocol specifications

Robert Siegmund, Dietmar Müller
June 2002 DAC '02: Proceedings of the 39th conference on Design automation
Publisher: ACM

Full text available: pdf(145.71 KB) Additional Information: full citation, abstract, references, cited by, index terms

An innovative methodology for the efficient design of communication controller hardware for popular protocols such as ATM, USB or CAN is proposed. In our approach, controller hardware in form of RTL models is synthesized from a formal specification of ...

Keywords: controller hardware synthesis, interface-based design, protocol specification

4 Compiler optimization of scalar value communication between speculative

threads
Antonia Zhai, Christopher B. Colohan, J. Gregory Steffan, Todd C. Mowry
December 2002 ACM SIGARCH Computer Architecture News, Volume 30 Issue 5
Publisher: ACM
Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, cited by

While there have been many recent proposals for hardware that supports *Thread-Level Speculation* (TLS), there has been relatively little work on compiler optimizations to fully exploit this potential for parallelizing programs optimistically. In ...

5 Thread-level parallelism and interactive performance of desktop applications
Kristián Flautner, Rich Uhlig, Steve Reinhardt, Trevor Mudge
November 2000 ASPLOS-IX: Proceedings of the ninth international conference on Architectural support for programming languages and operating systems
Publisher: ACM
Full text available: pdf(234.58 KB) Additional Information: full citation, abstract, references, cited by, index terms

Multiprocessing is already prevalent in servers where multiple clients present an obvious source of thread-level parallelism. However, the case for multiprocessing is less clear for desktop applications. Nevertheless, architects are designing processors ...

6 Design and performance evaluation of a web-based multi-tier federated system for a catalogue of life
Xuebiao Xu, Andrew C. Jones, W. Alex Gray, Nick J. Fiddian, Richard J. White, Frank A. Bisby
November 2002 WIDM '02: Proceedings of the 4th international workshop on Web information and data management
Publisher: ACM
Full text available: pdf(74.06 KB) Additional Information: full citation, abstract, references, index terms

In the SPICE (SPecies 2000 Interoperability Co-ordination Environment) project, we are designing and evaluating a web-based multi-tier federated system, intended as a scalable infrastructure for a globally distributed federated database of biological ...

Keywords: biodiversity informatics, caching, federated information system, multi-tier

7 Network performance modeling with NetArchitect ™ get a grip!
Michael A. Salsburg
March 1997 International Journal of Network Management, Volume 7 Issue 2
Publisher: John Wiley & Sons, Inc.
Full text available: pdf(876.89 KB) Additional Information: full citation, abstract, references, index terms

This article uses the traditional 'central server model' as a starting point and proposes additional abstractions to build an extended, 'non-central server' model. The model is implemented in a new product called NetArchitect ™. ...

8 When prefetching improves/degrades performance

Thomas R. Puzak, A. Hartstein, P. G. Emma, V. Srinivasan
May 2005 CF '05: Proceedings of the 2nd conference on Computing frontiers
Publisher: ACM

Full text available: pdf(161.60 KB) Additional Information: full citation, abstract, references, index terms

We formulate a new method for evaluating any prefetching algorithm (real or hypothetical). This method allows researchers to analyze the potential improvements prefetching can bring to an application independent of any known prefetching algorithm. We ...

Keywords: accuracy, cache, coverage, prefetch, prefetching algorithm, timeliness

9 Performance pathologies in hardware transactional memory

Jayaram Bobba, Kevin E. Moore, Haris Volos, Luke Yen, Mark D. Hill, Michael M. Swift, David A. Wood
June 2007 ACM SIGARCH Computer Architecture News, Volume 35 Issue 2
Publisher: ACM

Full text available: pdf(270.54 KB) Additional Information: full citation, abstract, references, index terms

Hardware Transactional Memory (HTM) systems reflect choices from three key design dimensions: conflict detection, version management, and conflict resolution. Previously proposed HTMs represent three points in this design space: lazy conflict detection, ...

Keywords: contention management, hardware, pathology, performance, transactional memory

10 Performance evaluation of adaptive MPI

Chao Huang, Gengbin Zheng, Laxmikant Kalé, Sameer Kumar
March 2006 PPoPP '06: Proceedings of the eleventh ACM SIGPLAN symposium on Principles and practice of parallel programming
Publisher: ACM

Full text available: pdf(399.56 KB) Additional Information: full citation, abstract, references, cited by, index terms

Processor virtualization via migratable objects is a powerful technique that enables the runtime system to carry out intelligent adaptive optimizations like dynamic resource management. Charm++ is an early language/system that supports migratable ...

Keywords: MPI, adaptivity, communication optimization, load balancing, processor virtualization

11 Automatic generation of performance models using the distributed management framework (DMF)

Asham El Rayess, Jerome A. Rolia
November 1997 CASCON '97: Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research
Publisher: IBM Press

Full text available: pdf(98.90 KB) Additional Information: full citation, abstract, references, index terms

The purpose of the Distributed Management Framework (DMF) is to provide a layer of abstraction at a level convenient for management application developers. Specifically, it liberates the management application developer from the need to deal with application-dependent ...

12 The price of performance

Luiz André Barroso
September 2005 Queue, Volume 3 Issue 7
Publisher: ACM

Full text available: pdf(180.88 KB) htm(20.67 KB) Additional Information: full citation, abstract, references, cited by, index terms

An economic case for chip multiprocessing.

13 Type inference for locality analysis of distributed data structures

Satish Chandra, Vijay Saraswat, Vivek Sarkar, Rastislav Bodik
February 2008 PPoPP '08: Proceedings of the 13th ACM SIGPLAN Symposium on Principles and practice of parallel programming
Publisher: ACM

Full text available: pdf(328.61 KB) Additional Information: full citation, abstract, references, index terms

In languages with distributed heap data structures, the type system typically conveys only coarse locality information: whether a reference is local or possibly remote. Often, of interest to the optimizing compiler or the user is a more fine-grain information, ...

Keywords: equality-based constraint system, partitioned global address space, type inference, unification, x10

14 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith
November 2003 ACM Transactions on Computer Systems (TOCS), Volume 21 Issue 4
Publisher: ACM

Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

15 Adaptive two-level thread management for fast MPI execution on shared memory machines

Kai Shen, Hong Tang, Tao Yang
January 1999 Supercomputing '99: Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM)
Publisher: ACM

Full text available: pdf(152.63 KB) Additional Information: full citation, references, cited by, index terms

16 A document object modeling method to retrieve data from a very large XML

document
Seung Min Kim, Suk I. Yoo, Eunji Hong, Tae Gwon Kim, Il Kon Kim
August 2007 DocEng '07: Proceedings of the 2007 ACM symposium on Document engineering
Publisher: ACM

Full text available: pdf(516.81 KB) Additional Information: full citation, abstract, references, index terms

Document Object Modeling (DOM) is widely used approach for retrieving data from an XML document. If the size of the XML document is very large, however, using the DOM approach for retrieving data from the XML document may suffer from a lack of memory ...

Keywords: DOM, DOM API, XML, very large XML documents

17 The efficiency of XML as an intermediate data representation for wireless middleware communication
Wayne Hanslo, Kenneth MacGregor
October 2004 SAICSIT '04: Proceedings of the 2004 annual research conference of the South African institute of computer scientists and information technologists on IT research in developing countries
Publisher: South African Institute for Computer Scientists and Information Technologists

Full text available: pdf(69.96 KB) Additional Information: full citation, abstract, references, index terms

Along with the advances in networking technologies, access to data services from mobile devices is growing in popularity but many issues have to be considered when writing applications for mobile devices. Devices have limited resources and wireless networks ...

Keywords: SOAP, XML, design, measurement, middleware, mobile computing, performance, wireless

18 Experiences in Design and Implementation of a High Performance Transport Protocol
Yunhong Gu, Xinwei Hong, Robert L. Grossman
November 2004 SC '04: Proceedings of the 2004 ACM/IEEE conference on Supercomputing
Publisher: IEEE Computer Society

Full text available: pdf(193.37 KB) Additional Information: full citation, abstract, references, cited by

This paper describes our experiences in the development of the UDP-based Data Transport (UDT) protocol, an application level transport protocol used in distributed data intensive applications. The new protocol is motivated by the emergence of wide area ...

Keywords: Performance, Design, Experimentation, UDT, transport protocol, data intensive application, design, implementation

19 Exploratory sequential data analysis: exploring continuous observational data
Carolanne Fisher, Penelope Sanderson
March 1996 interactions, Volume 3 Issue 2
Publisher: ACM

Full text available: pdf(680.05 KB) Additional Information: full citation, references, cited by, index terms, review

20

Online optimizations driven by hardware performance monitoring
Florian T. Schneider, Mathias Payer, Thomas R. Gross
June 2007 PLDI '07: Proceedings of the 2007 ACM SIGPLAN conference on Programming language design and implementation
Publisher: ACM

Full text available: pdf(224.36 KB) Additional Information: full citation, abstract, references, index terms

Hardware performance monitors provide detailed direct feedback about application behavior and are an additional source of infor-mation that a compiler may use for optimization. A JIT compiler is in a good position to make use of such information because ...

Keywords: Java, dynamic optimization, hardware performance monitors, just-in-time compilation

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